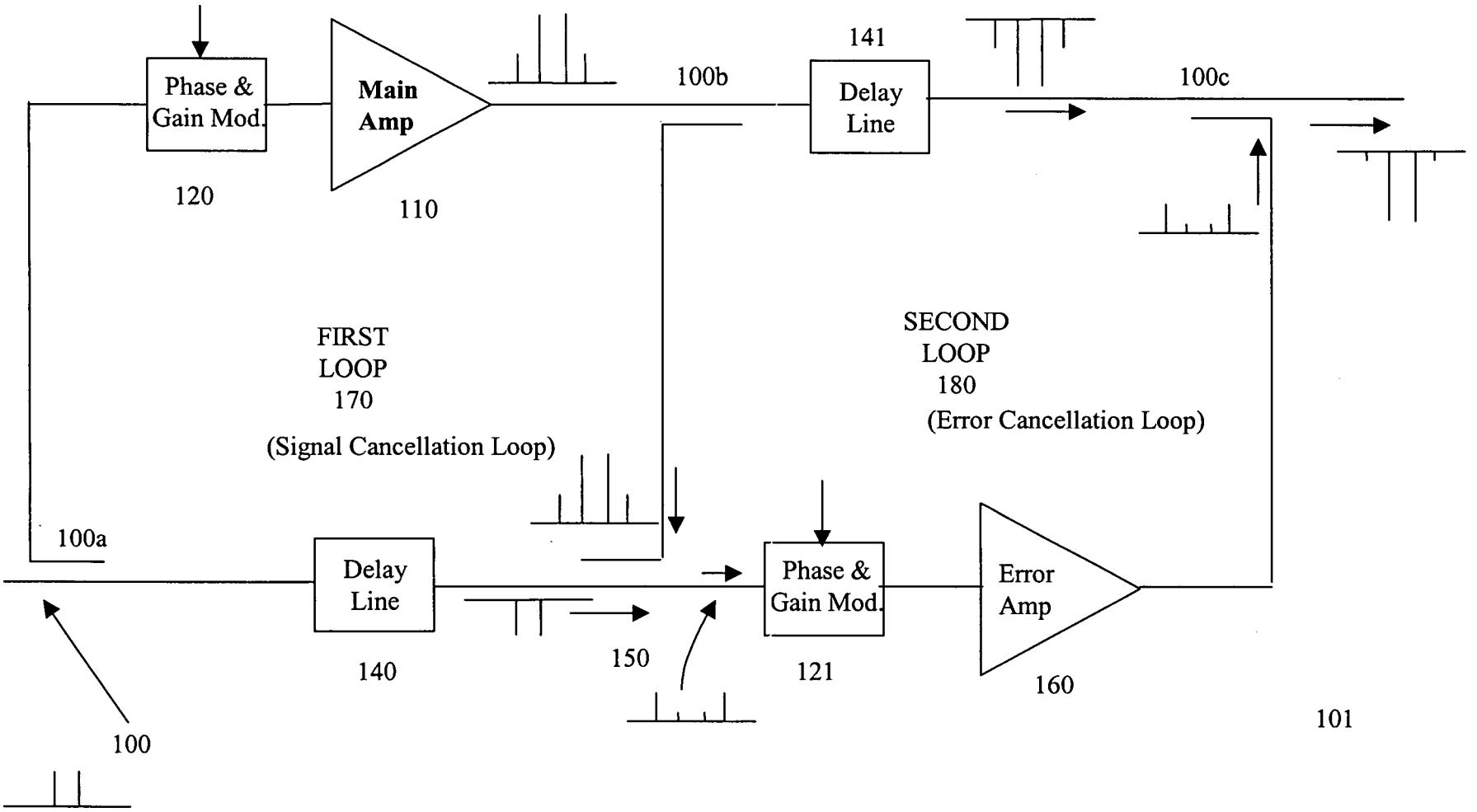

PRIOR ART

FIG. 1

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Informal Drawings

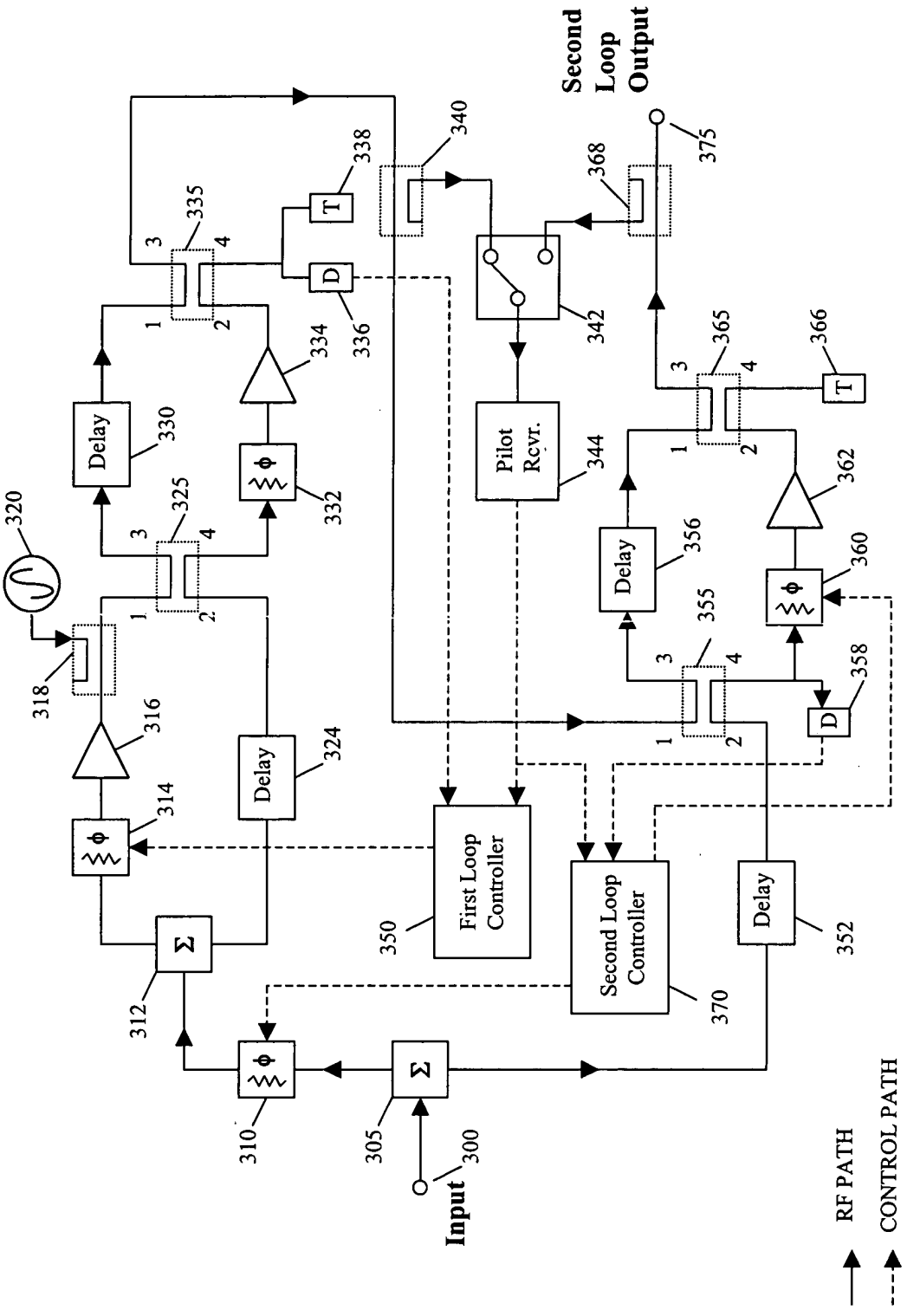
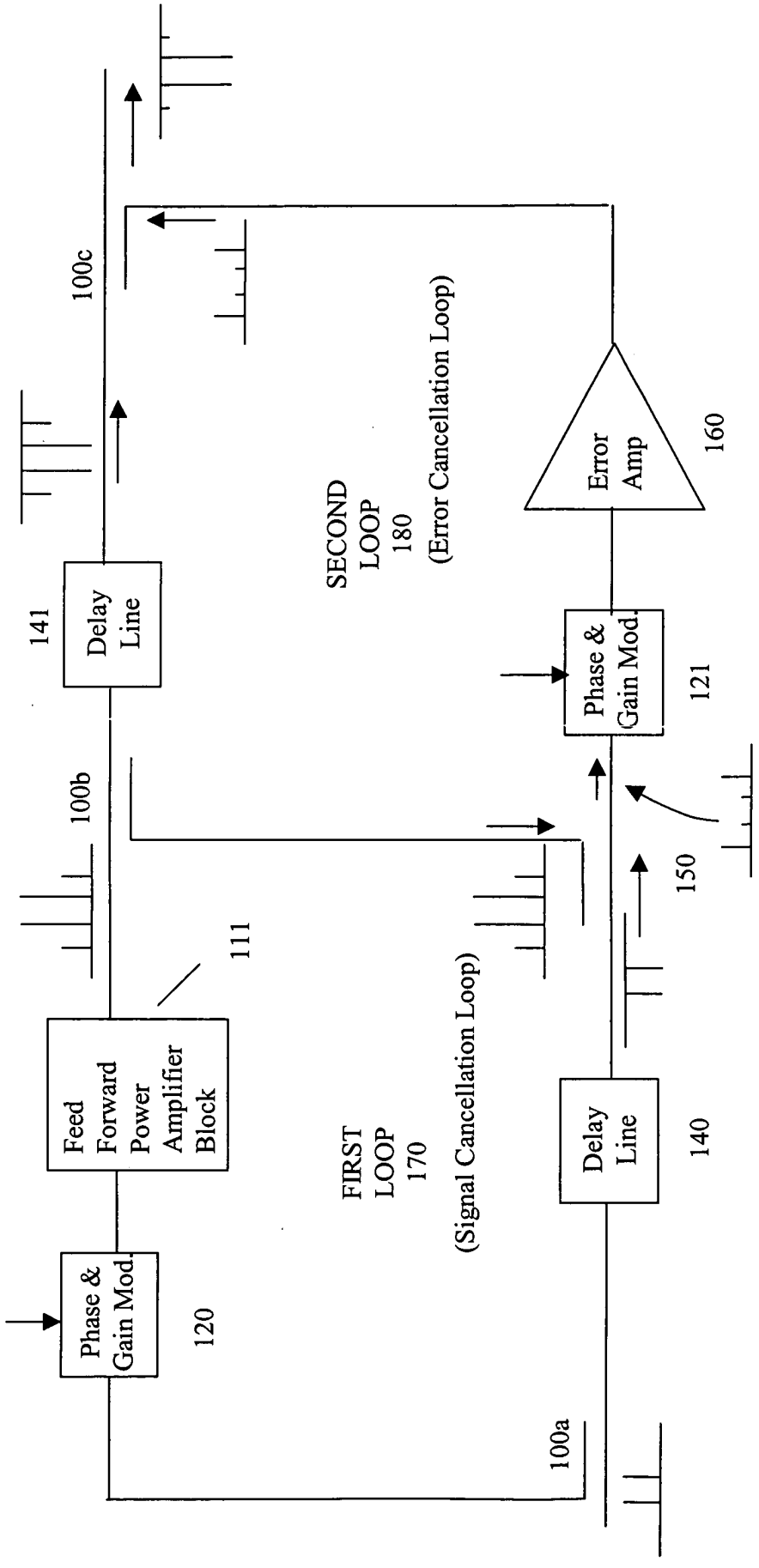


FIG. 2

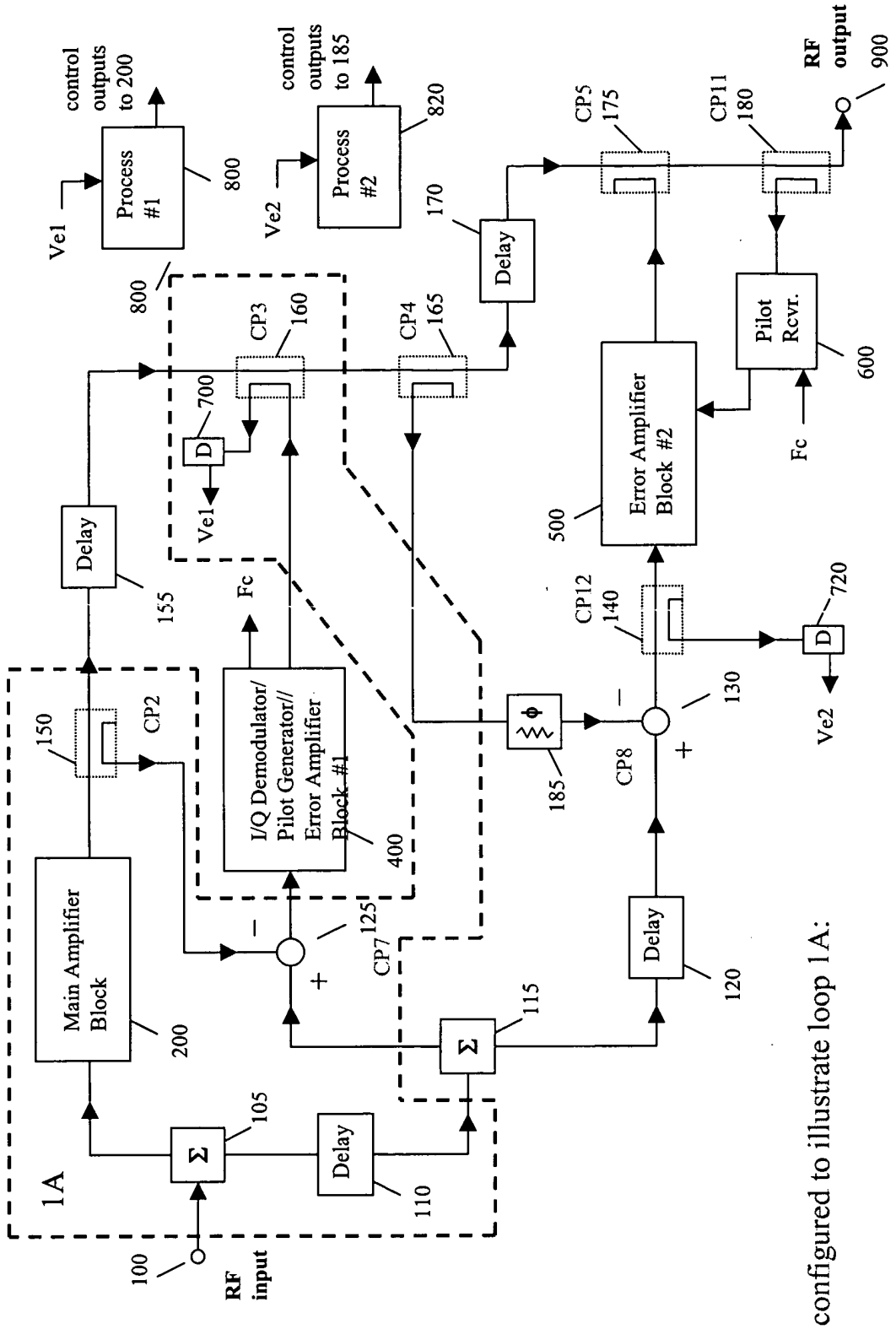
PRIOR ART

Originally Filed
Informal Drawings



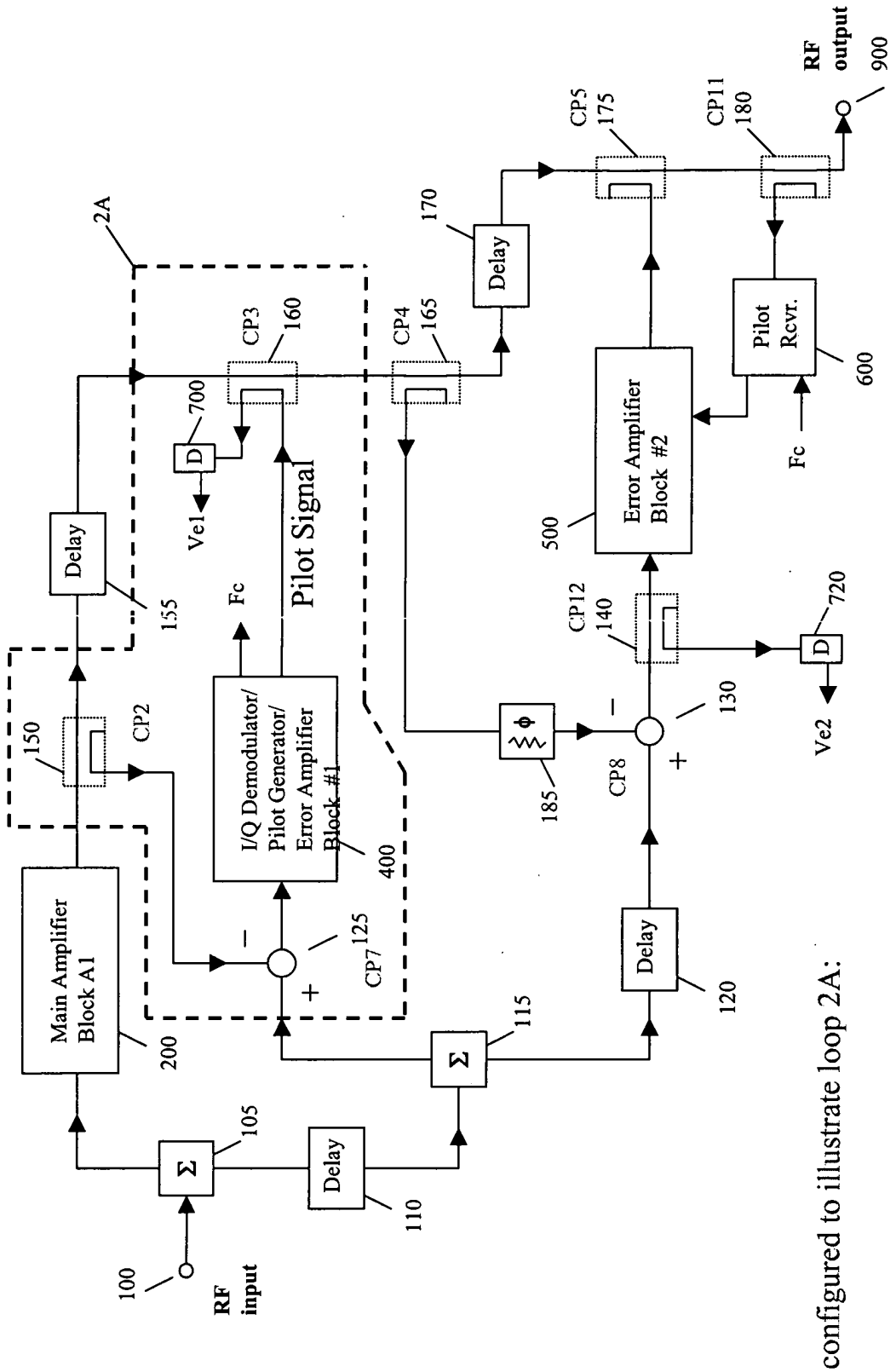
PRIOR ART

FIG. 3



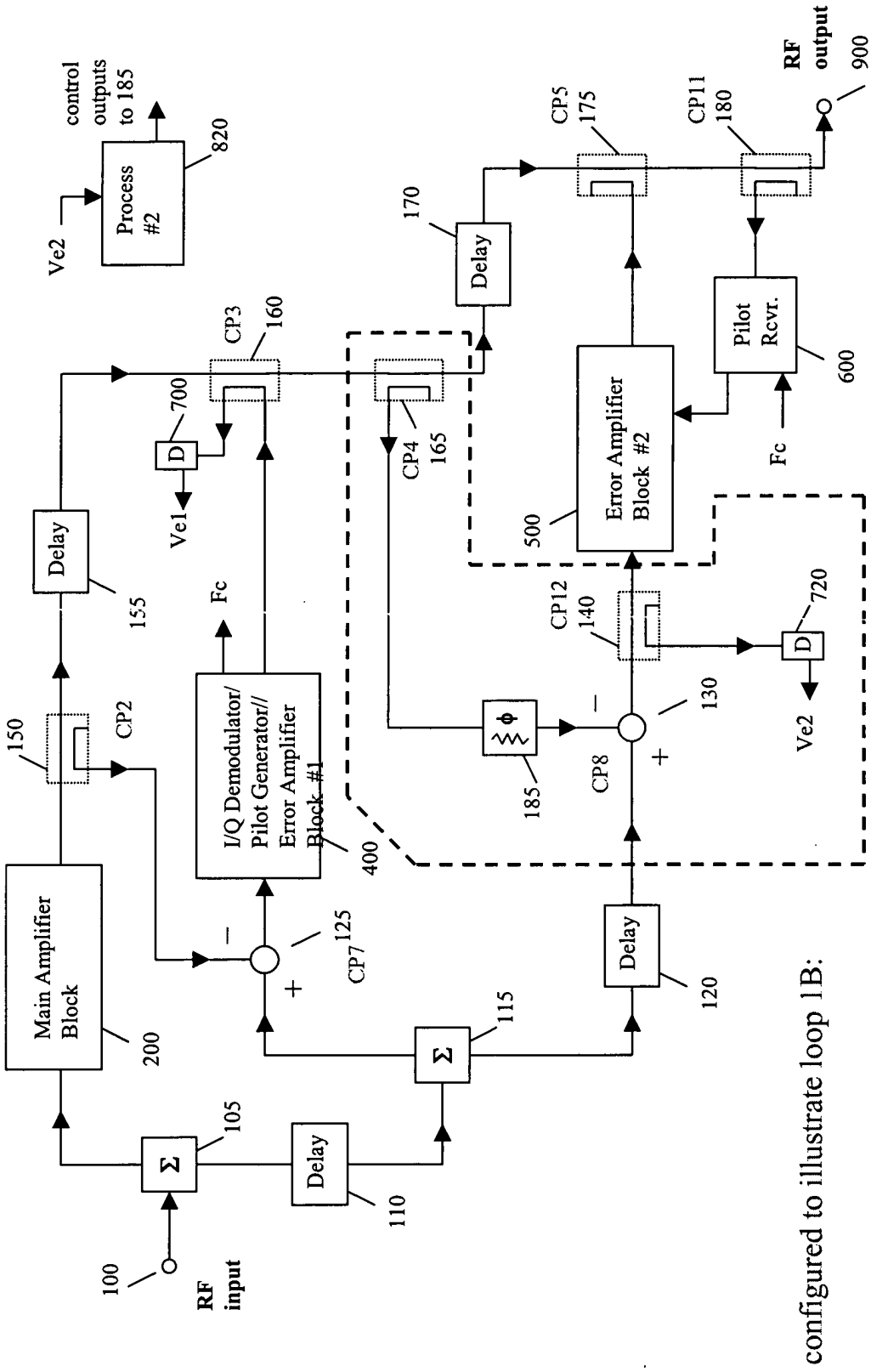
configured to illustrate loop 1A:

FIG. 4



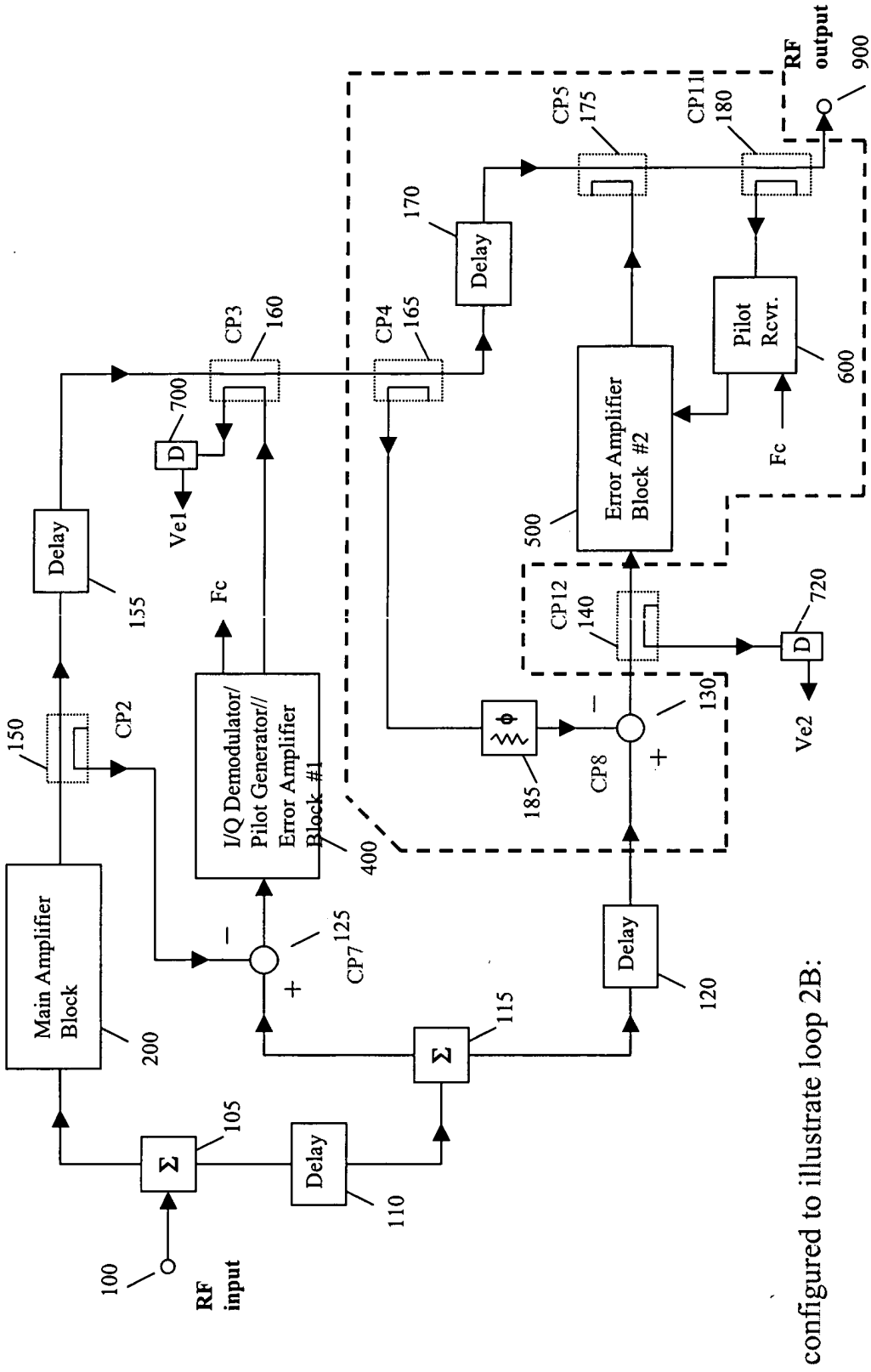
configured to illustrate loop 2A:

FIG. 5



configured to illustrate loop 1B:

FIG. 6



configured to illustrate loop 2B:

FIG. 7

Originally Filed
Informal Drawings

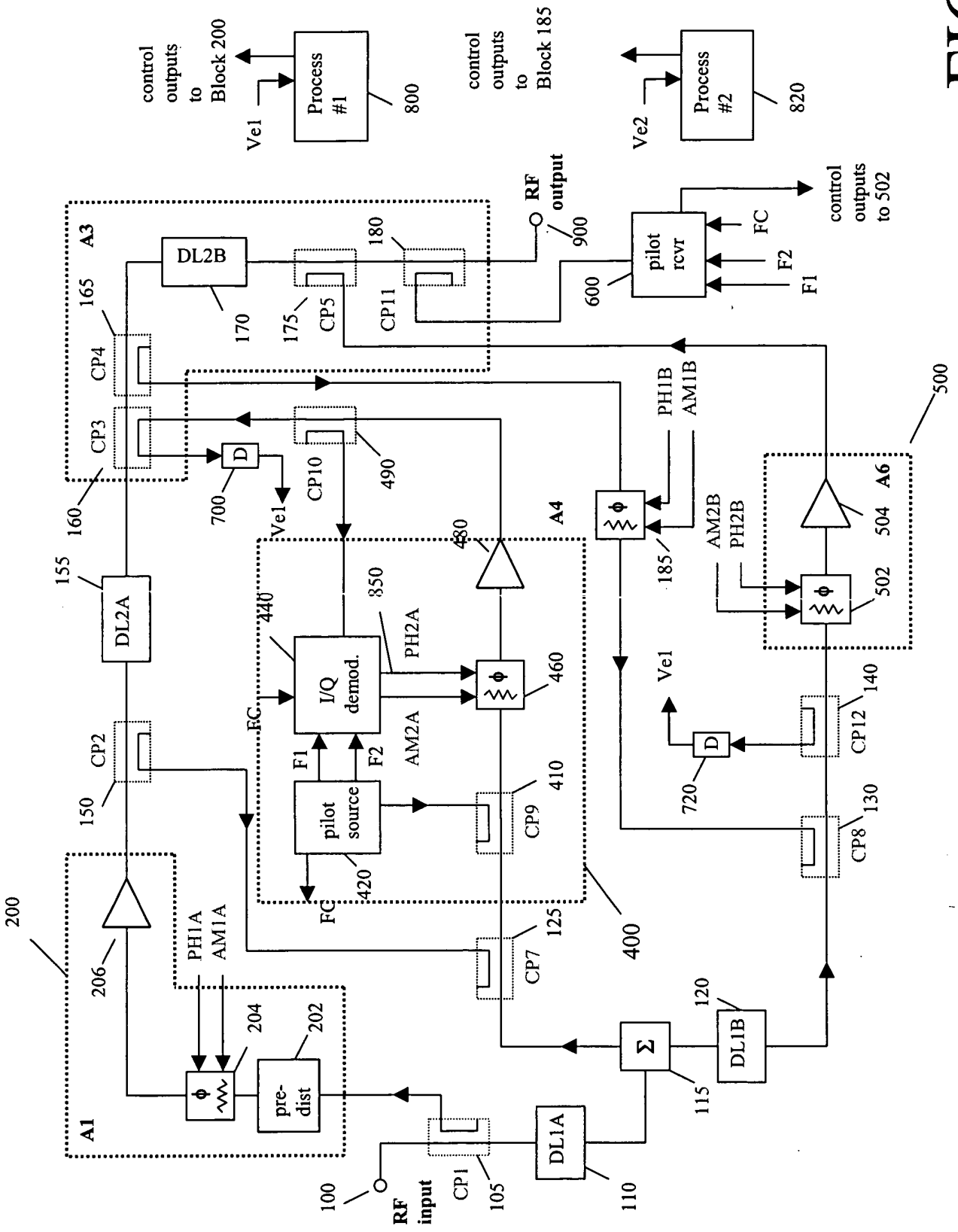


FIG. 8

FIG. 9

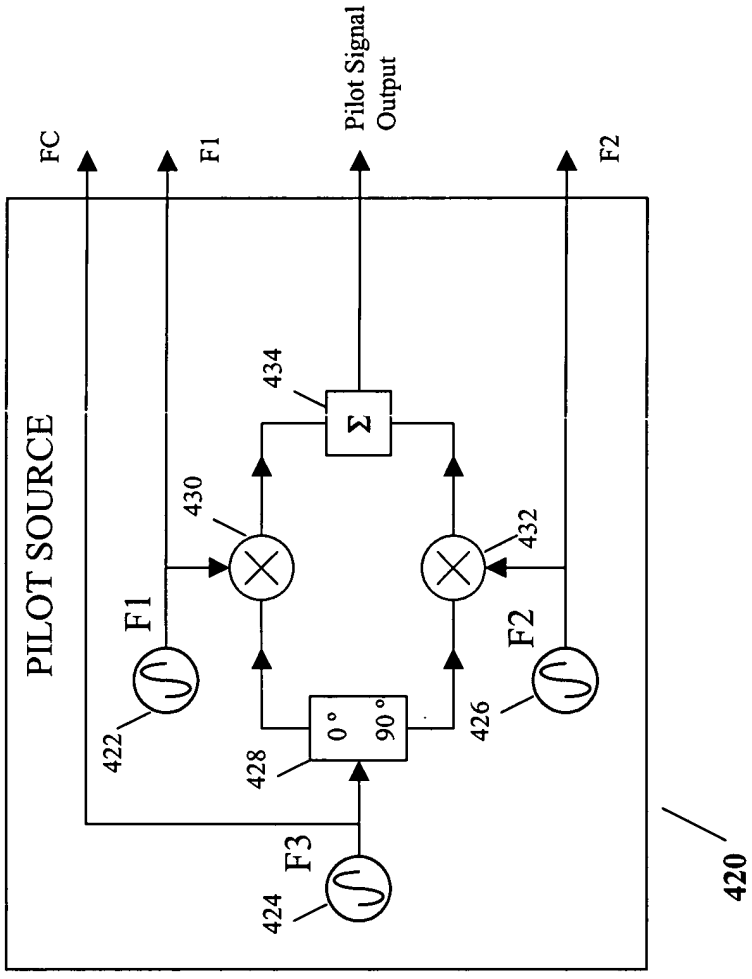
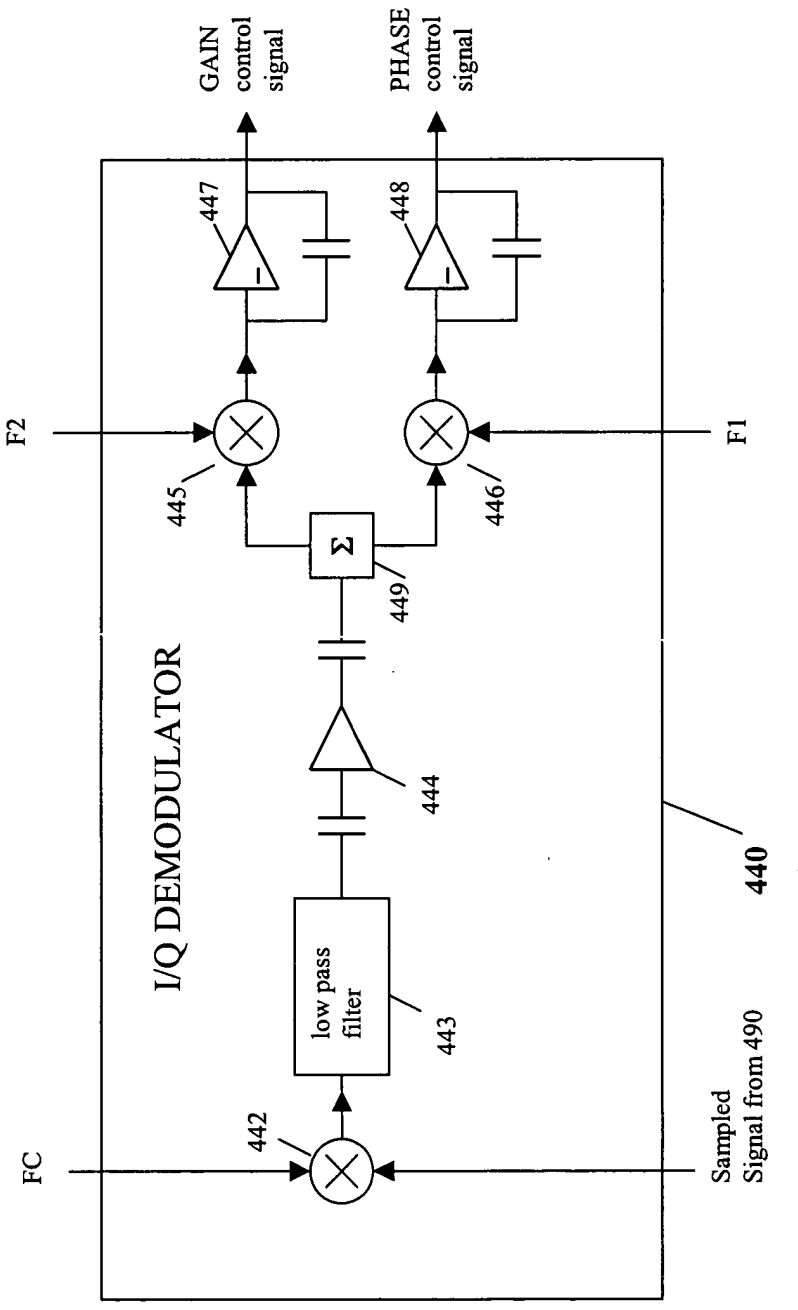

PILOT SOURCE
FC
F1
Pilot Signal Output
F2
434
Σ
430
432
F1
F2
422
428
0 °
90 °
426
F3
424
420

FIG. 10


GAIN control signal
PHASE control signal
447
448
F2
F1
445
446
Σ
449
I/Q DEMODULATOR
444
low pass filter
443
442
FC
Sampled Signal from 490
440

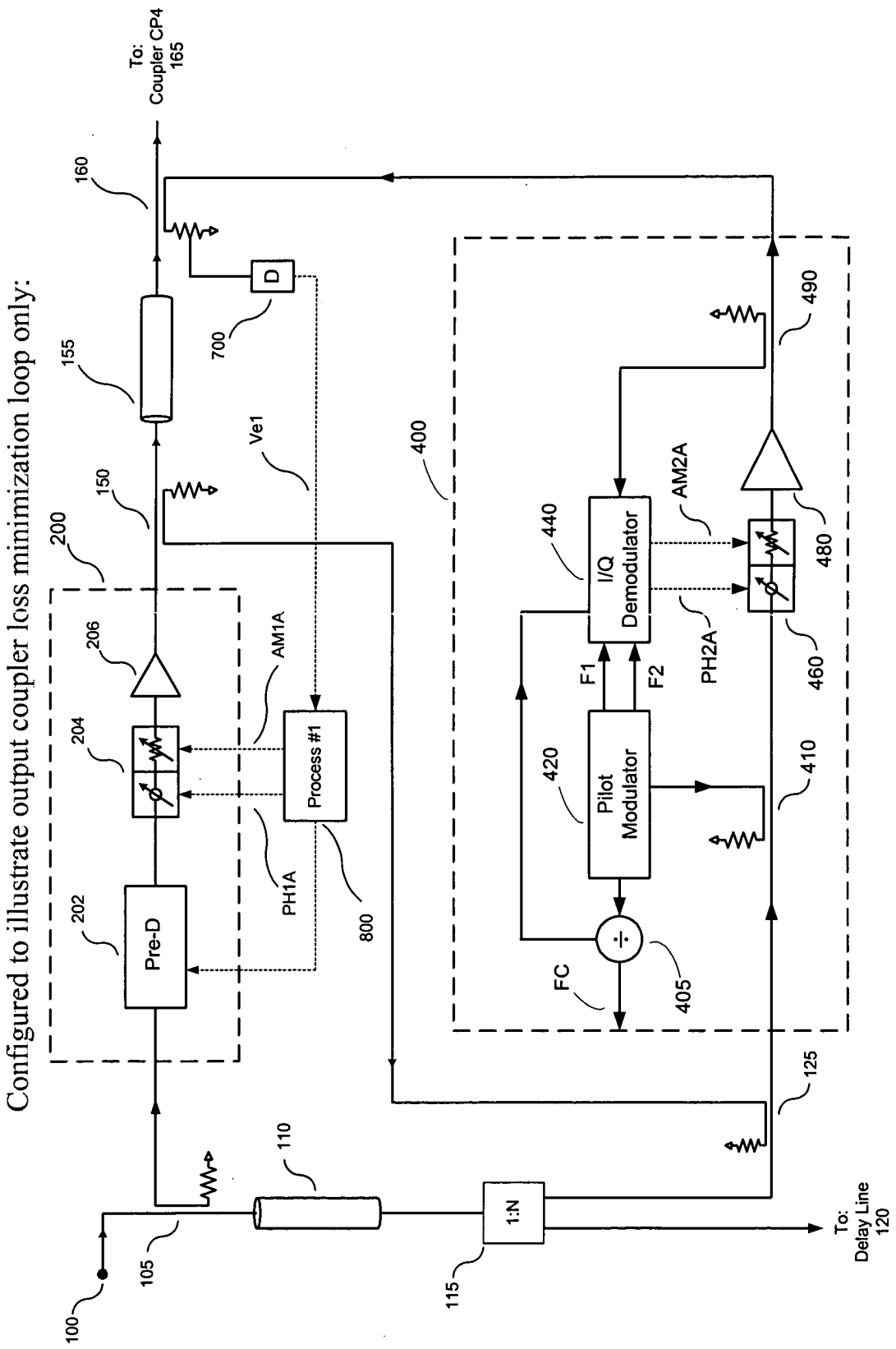

Configured to illustrate output coupler loss minimization loop only:
To: Coupler CP4 165
160
155
150
200
206
204
202
Pre-D
PH1A
AM1A
Process #1
800
Ve1
700
D
400
440
I/Q Demodulator
AM2A
PH2A
F1
F2
420
Pilot Modulator
FC
405
490
480
460
410
125
110
105
100
115
1:N
To: Delay Line 120

FIG. 11

Originally Filed
Informal Drawings

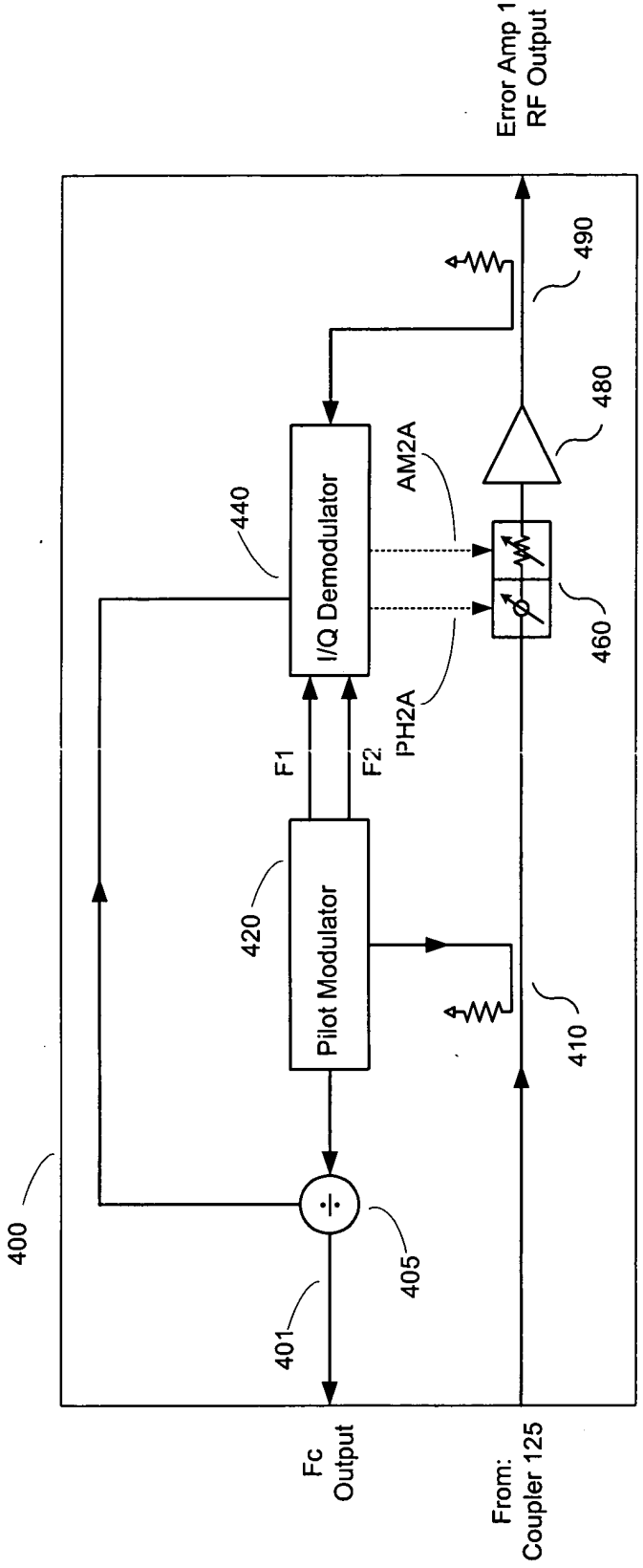


FIG. 12

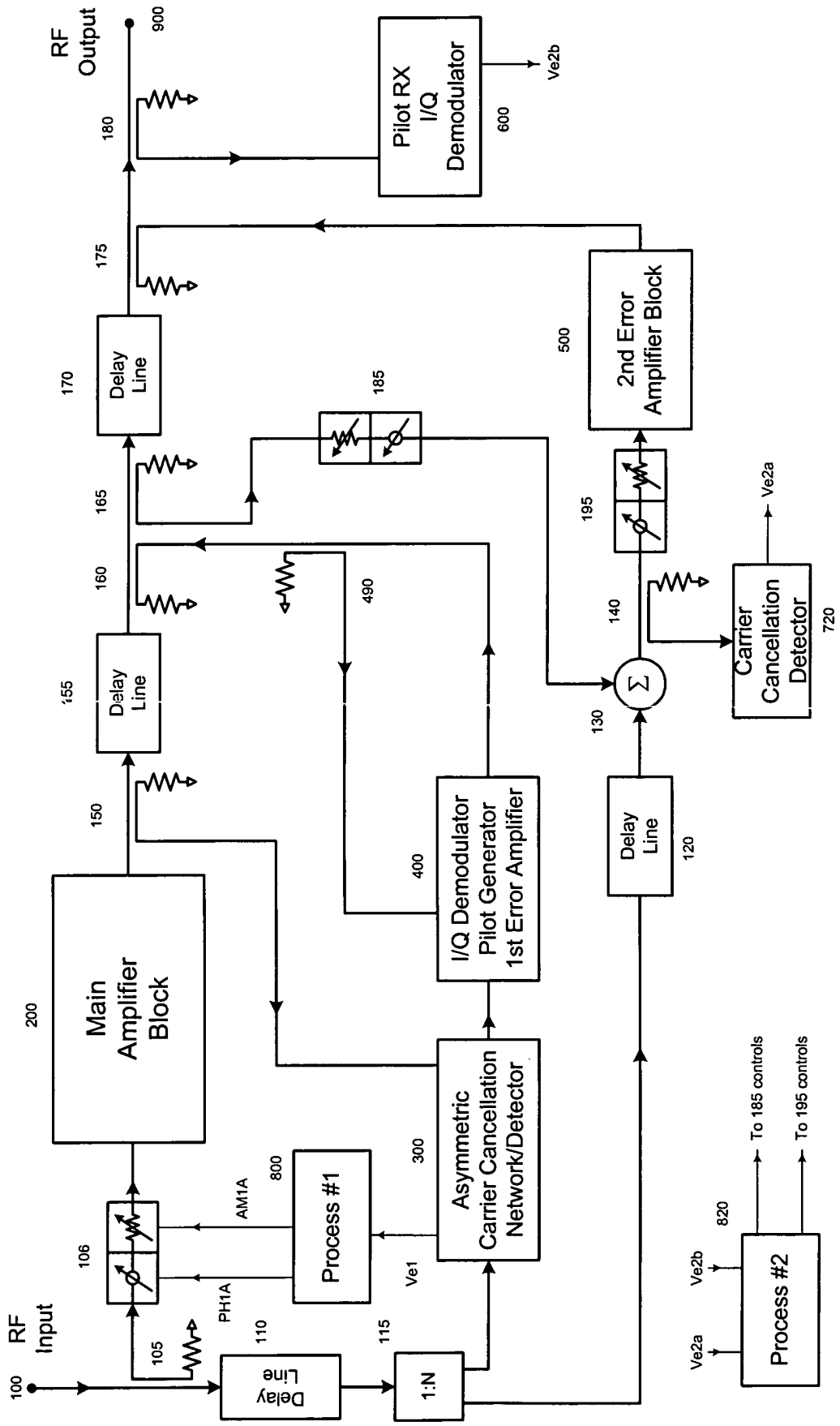

RF Input
100
105
106
110
PH1A
AM1A
800
Process #1
Delay Line
1:N
115
Ve1
300
Asymmetric Carrier Cancellation Network/Detector
400
I/Q Demodulator Pilot Generator 1st Error Amplifier
200
Main Amplifier Block
150
155
Delay Line
160
165
Delay Line
170
175
180
RF Output
900
Pilot RX I/Q Demodulator
600
Ve2b
185
490
500
2nd Error Amplifier Block
195
140
130
Σ
Delay Line
120
Carrier Cancellation Detector
720
Ve2a
Ve2b
Ve2a
820
Process #2
To 185 controls
To 195 controls

FIG. 13A

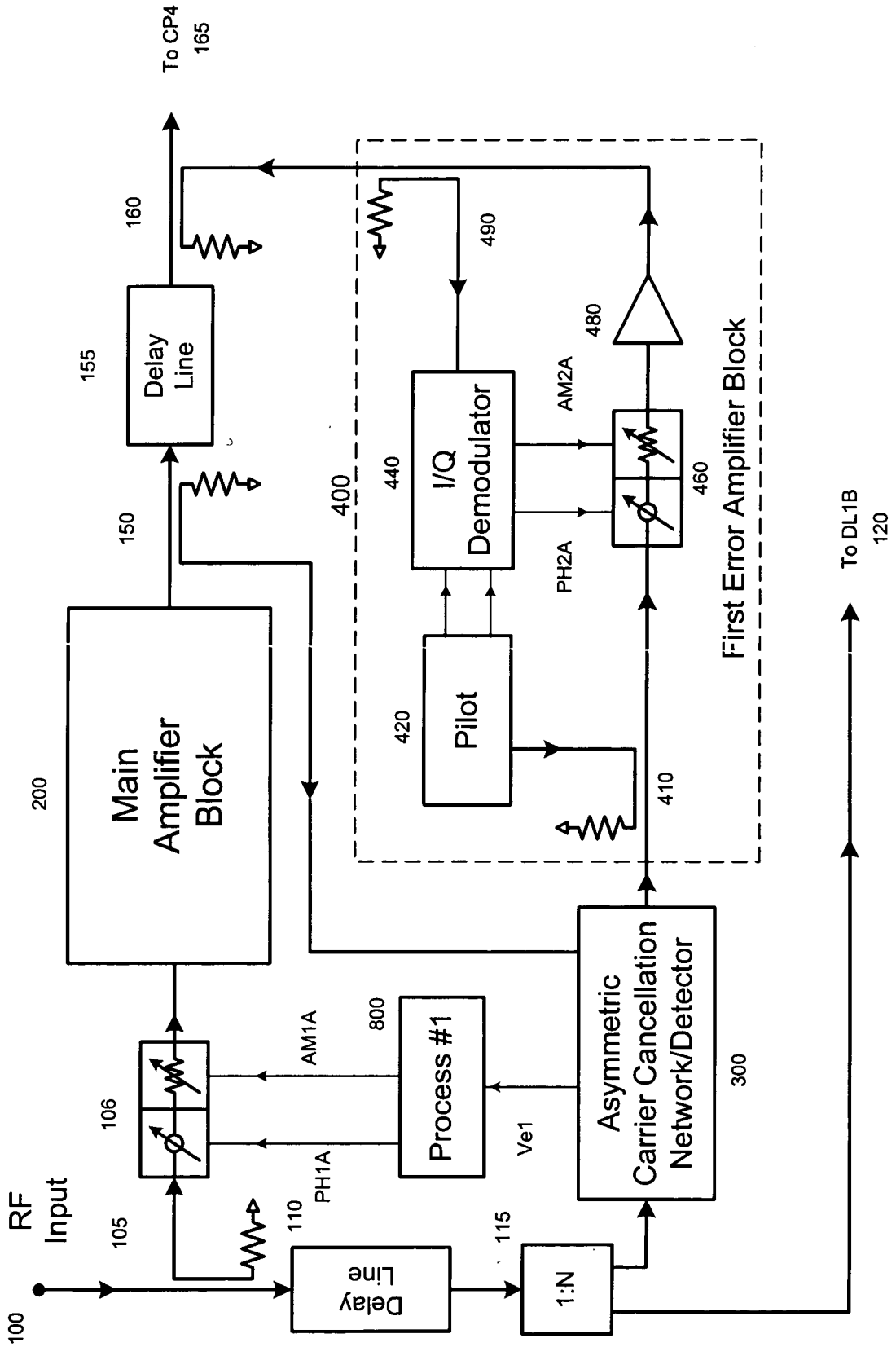

RF Input
100
105
106
AM1A
PH1A
800
Process #1
Ve1
110
Delay Line
115
1:N
Asymmetric Carrier Cancellation Network/Detector
300
To DL1B
120
200
Main Amplifier Block
150
155
Delay Line
160
To CP4
165
400
First Error Amplifier Block
410
420
Pilot
440
I/Q Demodulator
490
AM2A
PH2A
460
480

FIG. 13B

Originally Filed
Informal Drawings

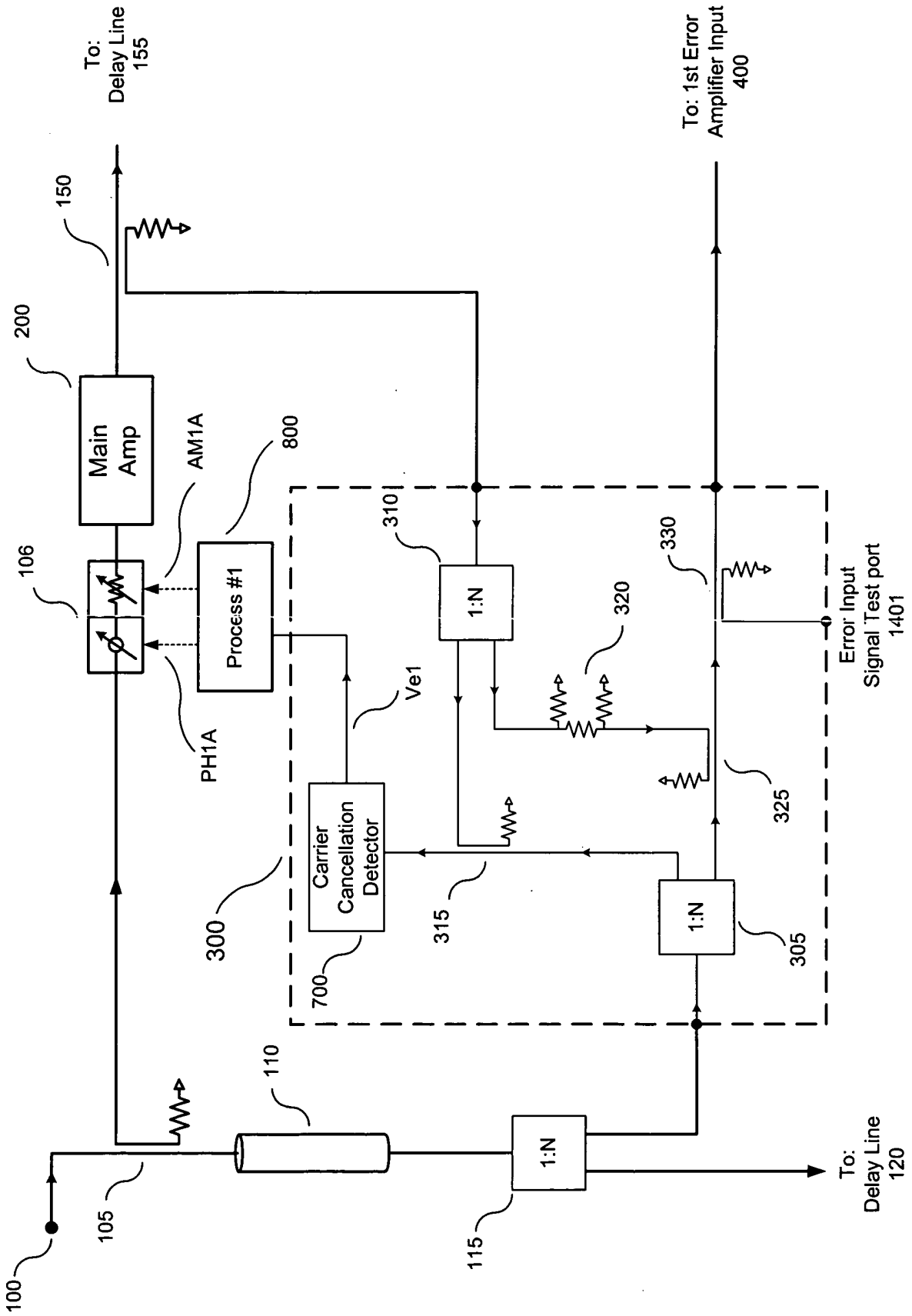


FIG. 14

Originally Filed
Informal Drawings

1st Error Amplifier Stabilization

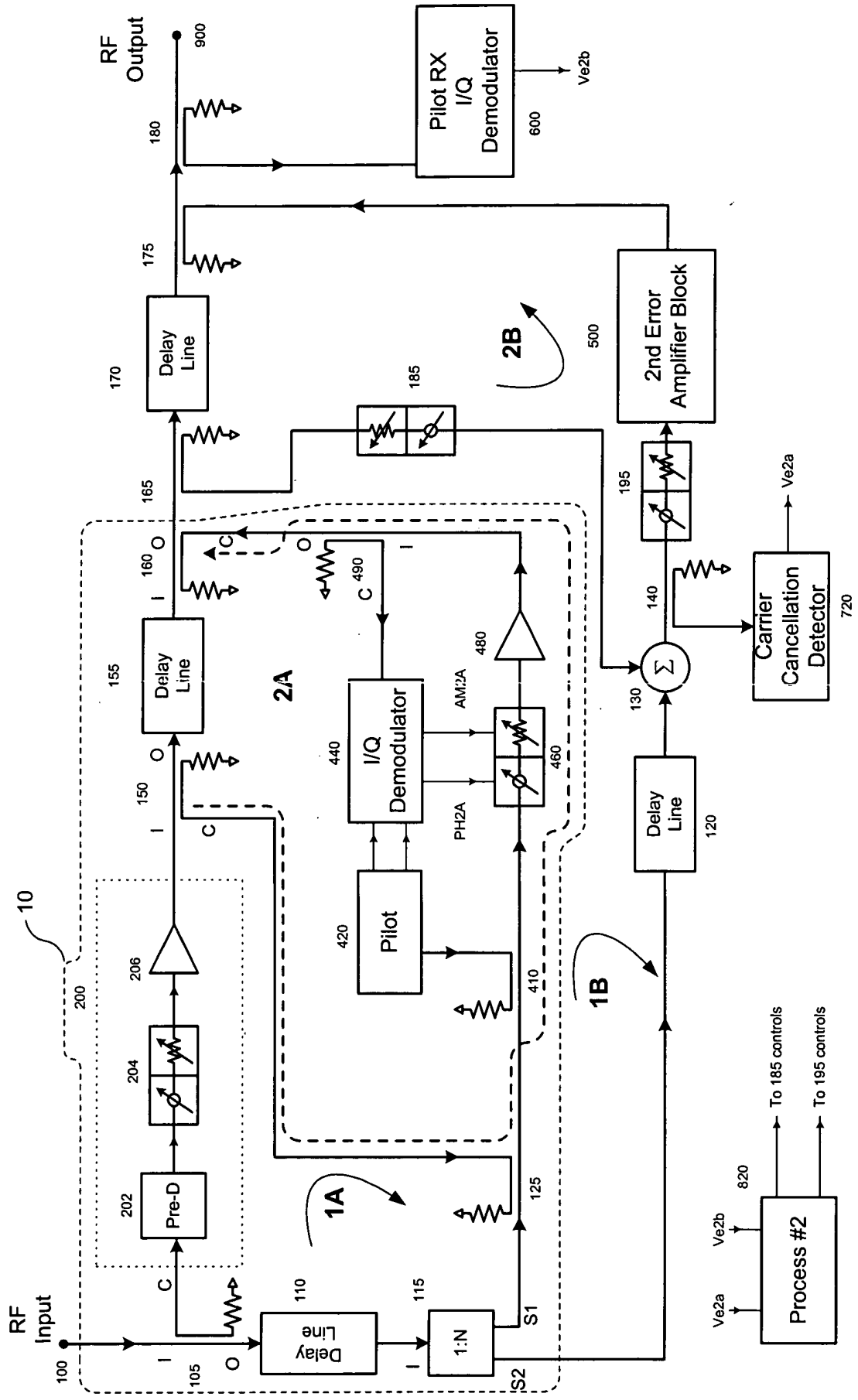
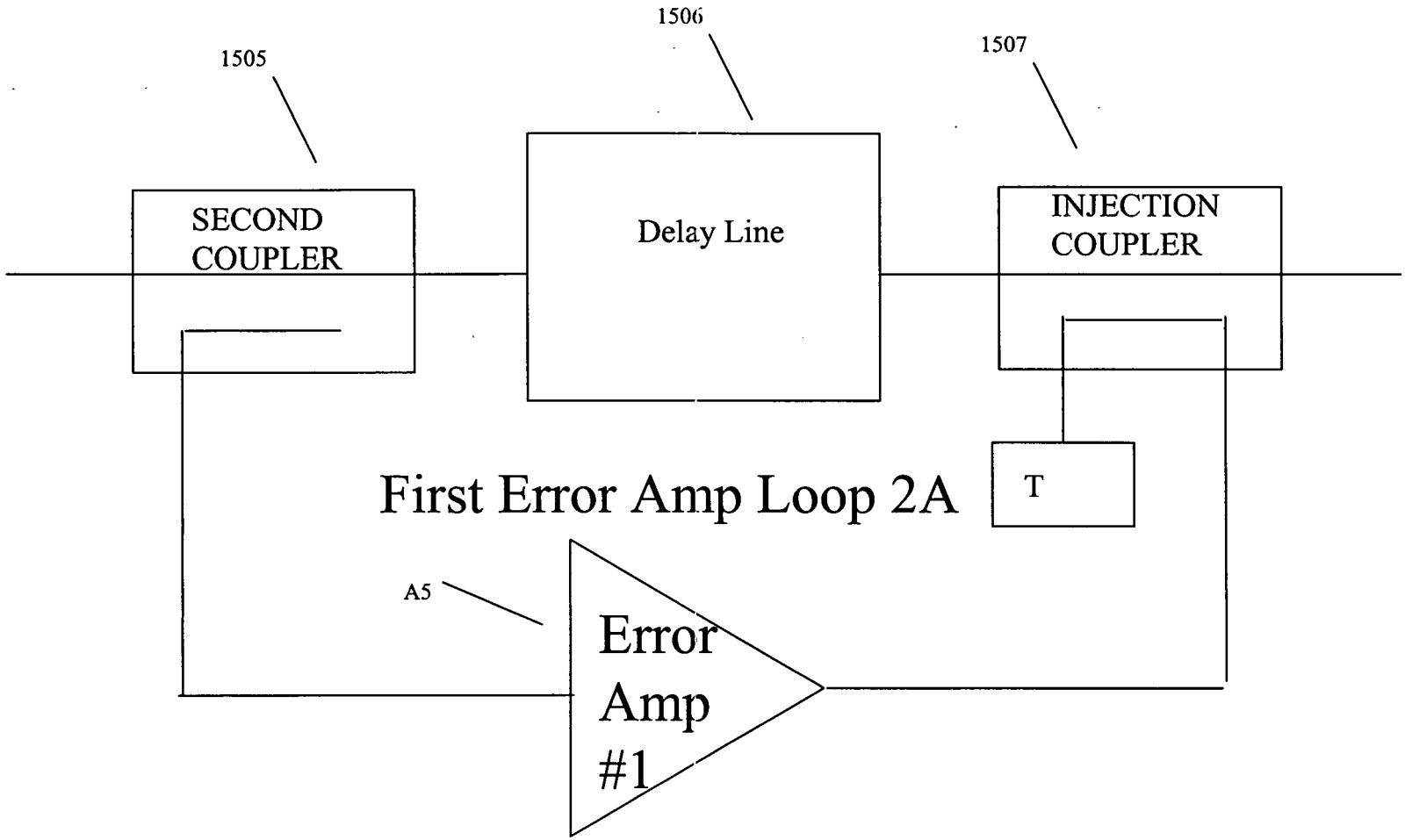


FIG. 15

Error Amplifier Stabilization



Originally Filed Informal Drawings

FIG. 16

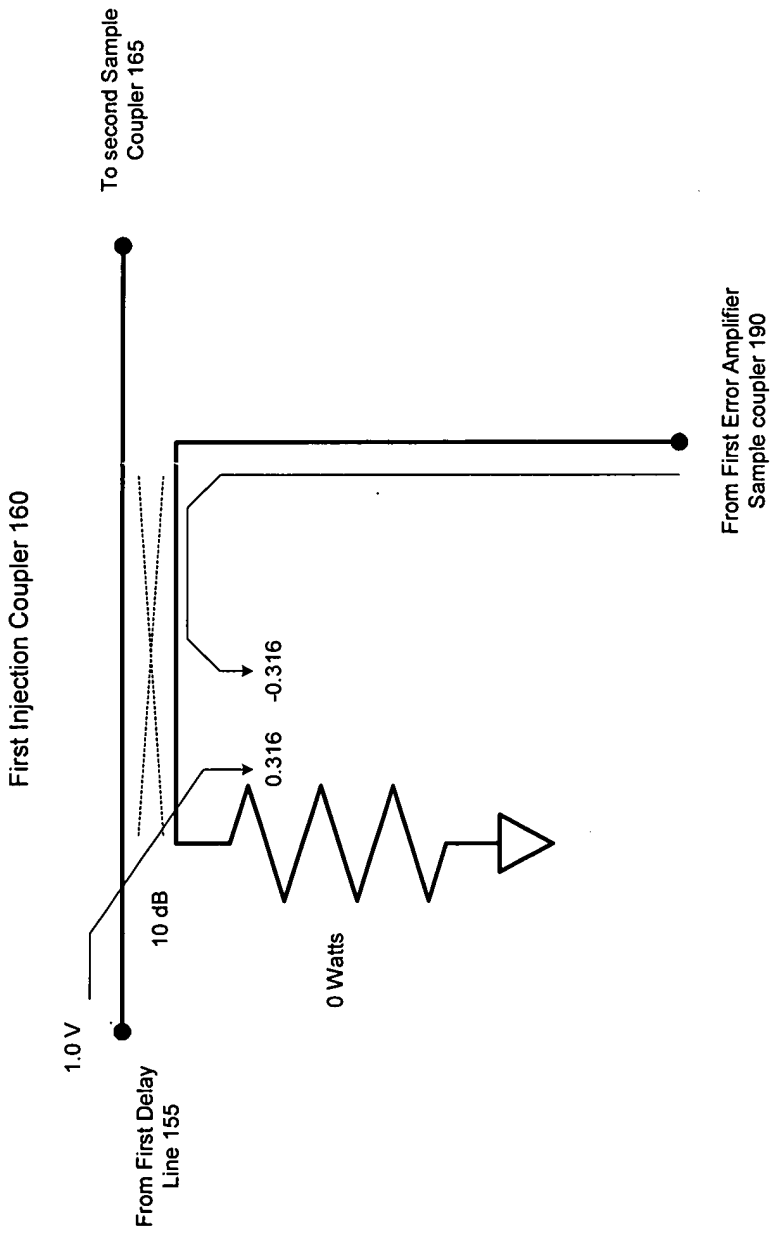

To second Sample Coupler 165
First Injection Coupler 160
From First Error Amplifier Sample coupler 190
-0.316
0.316
10 dB
0 Watts
1.0 V
From First Delay Line 155

FIG. 17

Originally Filed
Informal Drawings

Carrier Re-Injection

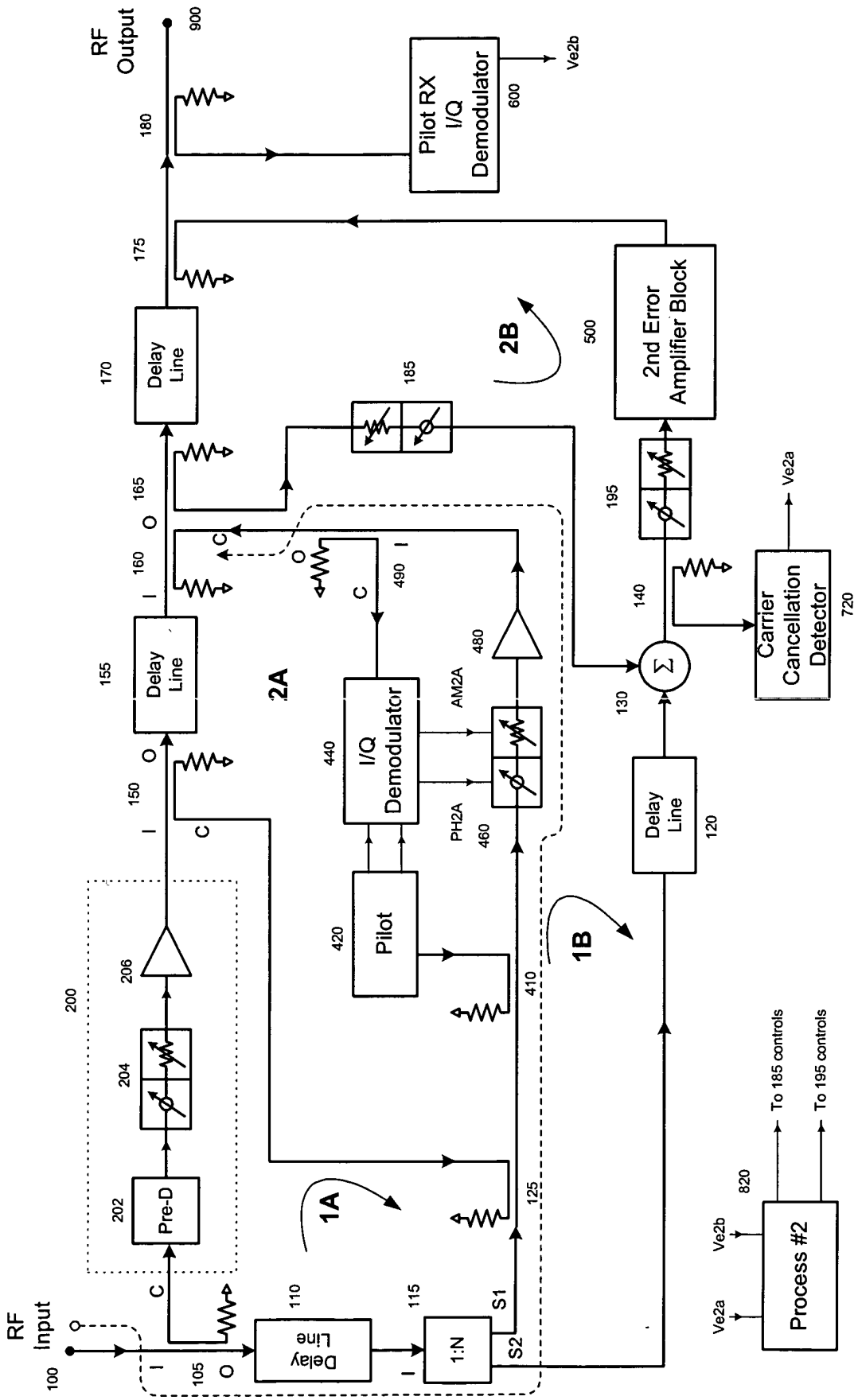


FIG. 18

Non-Overlapping Loop Adjustment

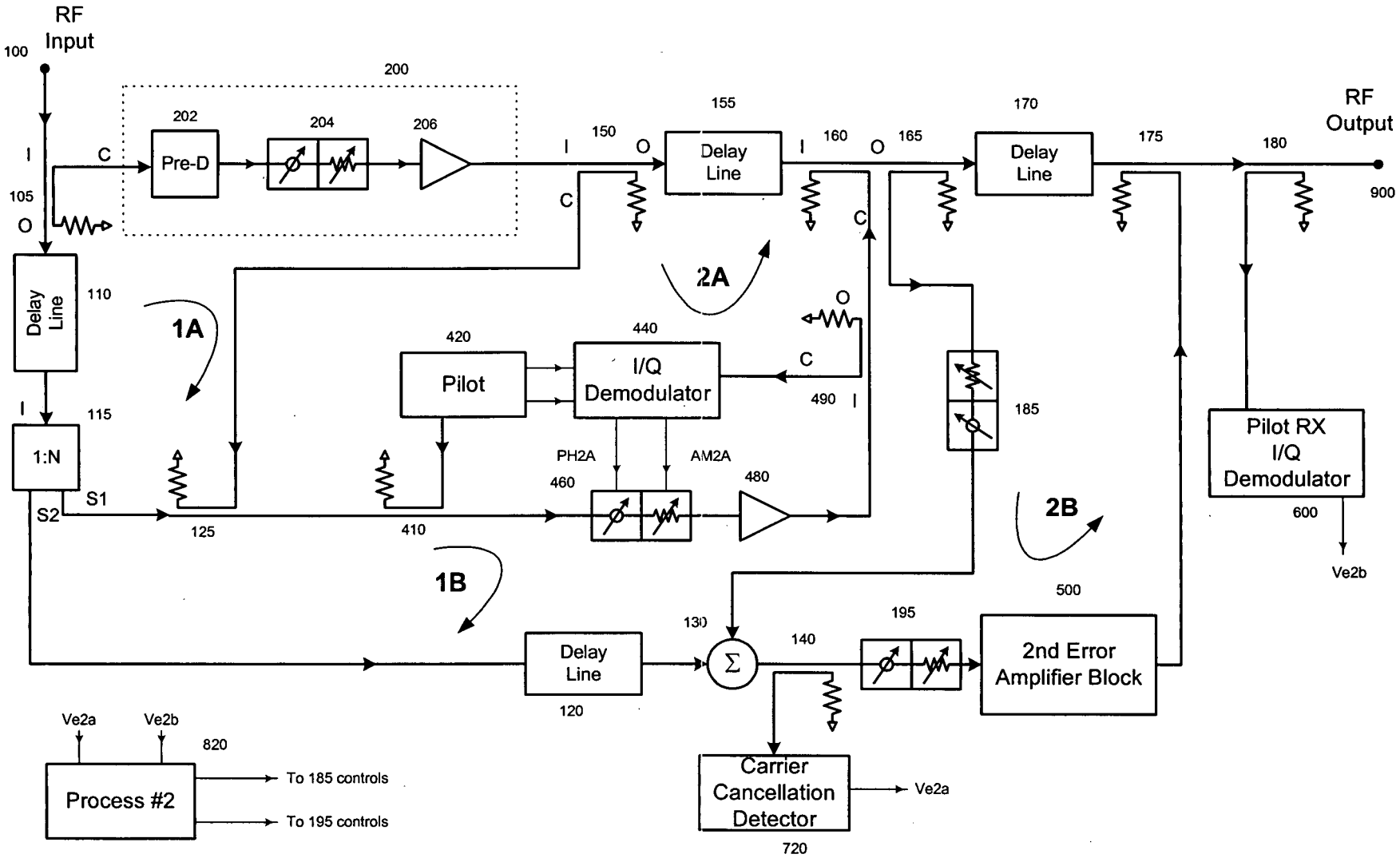


FIG. 19